

Fig. 1A (Prior Art)

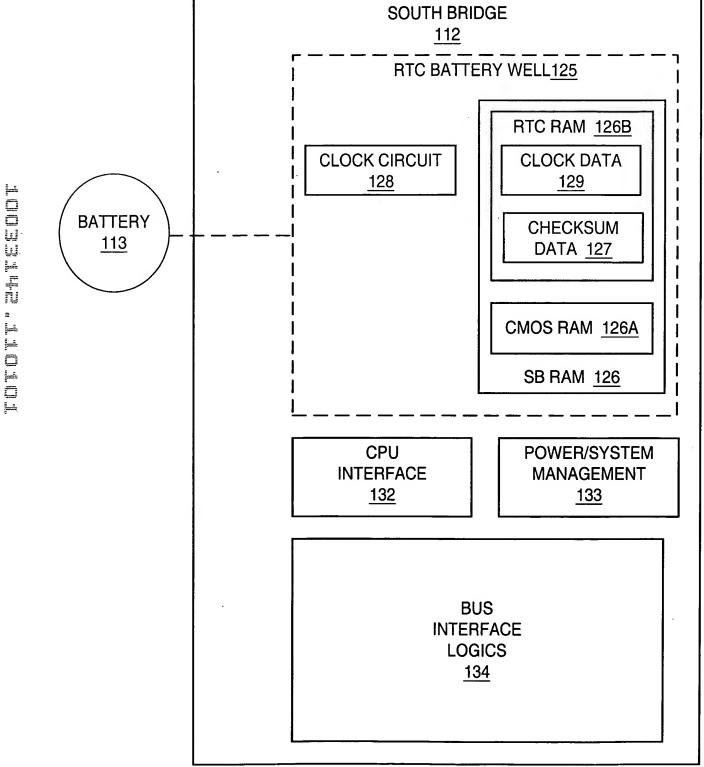


Fig. 1B (Prior Art)

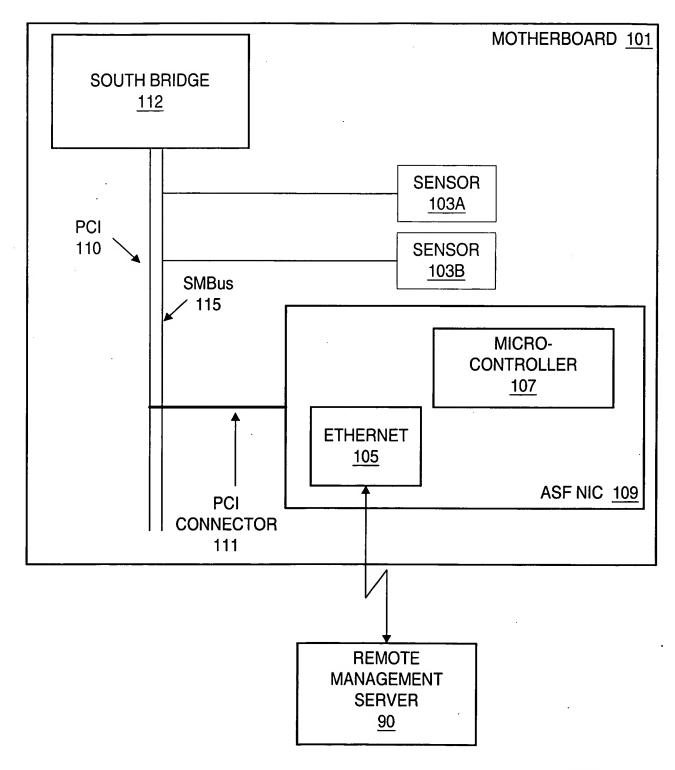


Fig. 1C (Prior Art)

POWER SUPPLY INITIALIZATION POWER SUPPLY GENERATES A POWER GOOD SIGNAL TO THE NORTH BRIDGE 136

UPON RECEIVING THE POWER GOOD SIGNAL, THE SOUTH BRIDGE STOPS
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THE PROCESSOR READS THE DEFAULT JUMP LOCATION, USUALLY AT FFFF0h 140

THE PROCESSOR JUMPS TO THE BIOS CODE LOCATION IN THE ROM BIOS, COPIES THE BIOS CODE TO RAM, AND BEGINS PROCESSING BIOS CODE INSTRUCTIONS FROM RAM 142

BIOS CODE PERFORMS POWER ON SELF TEST (POST) 144

BIOS CODE LOOKS FOR ADDITIONAL BIOS CODE, SUCH AS VIDEO @ C000h AND ATA/IDE HARD DRIVE BIOS CODE @ C800h, AND DISPLAYS A START-UP INFORMATION SCREEN 146

BIOS CODE PERFORMS ADDITIONAL SYSTEM TESTS, SUCH AS THE RAM COUNT-UP TEST, AND SYSTEM INVENTORY, SUCH AS IDENTIFYING COM AND LPT PORTS AND INITIALIZING THE ASF NIC 148

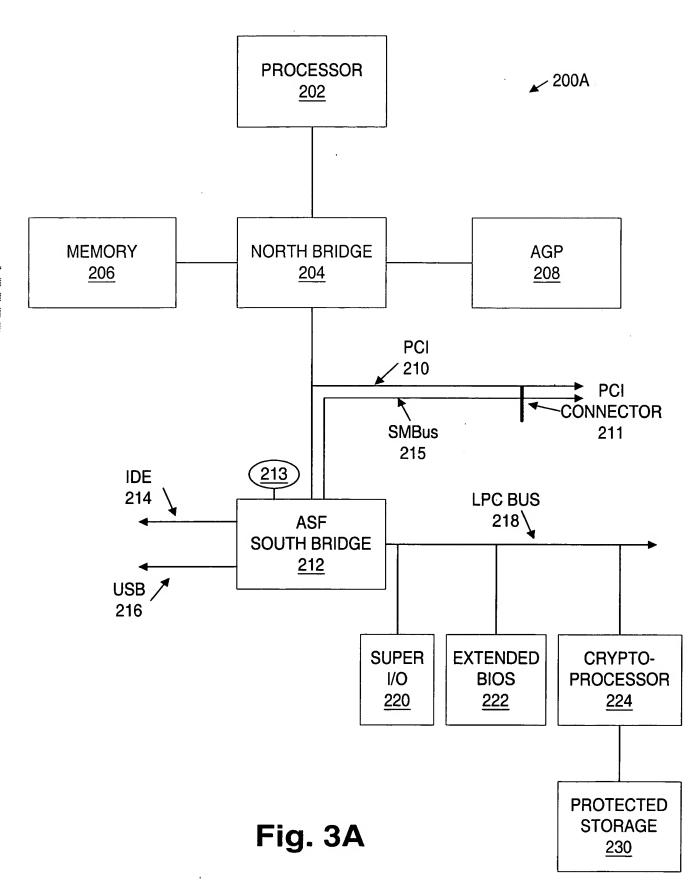
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BIOS CODE IDENTIFIES THE BOOT LOCATION 152

BIOS CODE CALLS THE BOOT SECTOR CODE TO BOOT THE COMPUTER SYSTEM 154

Fig. 2 (Prior Art)

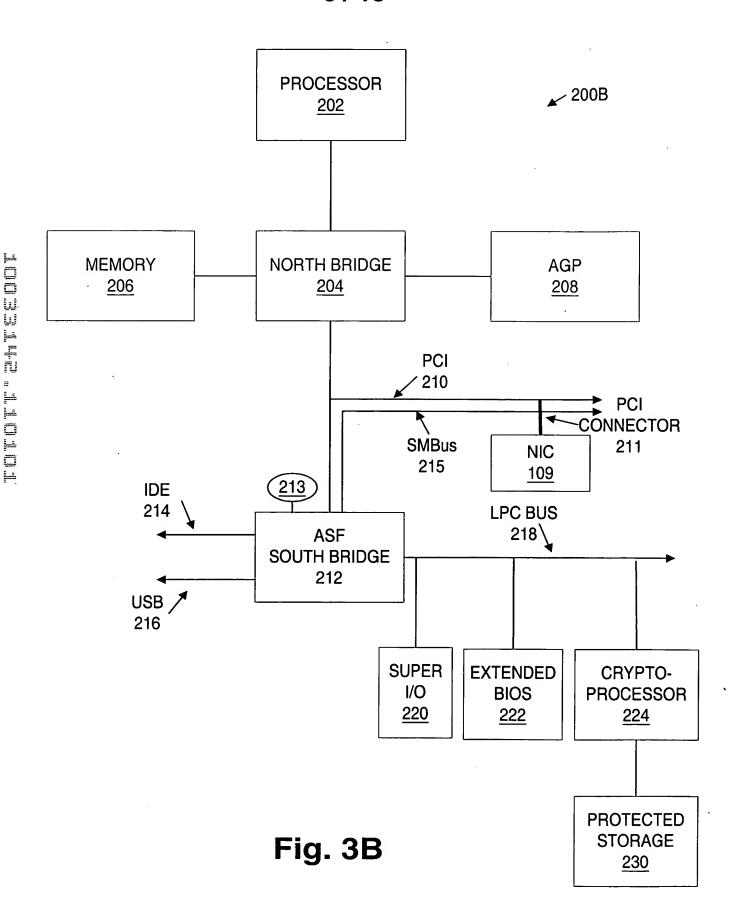




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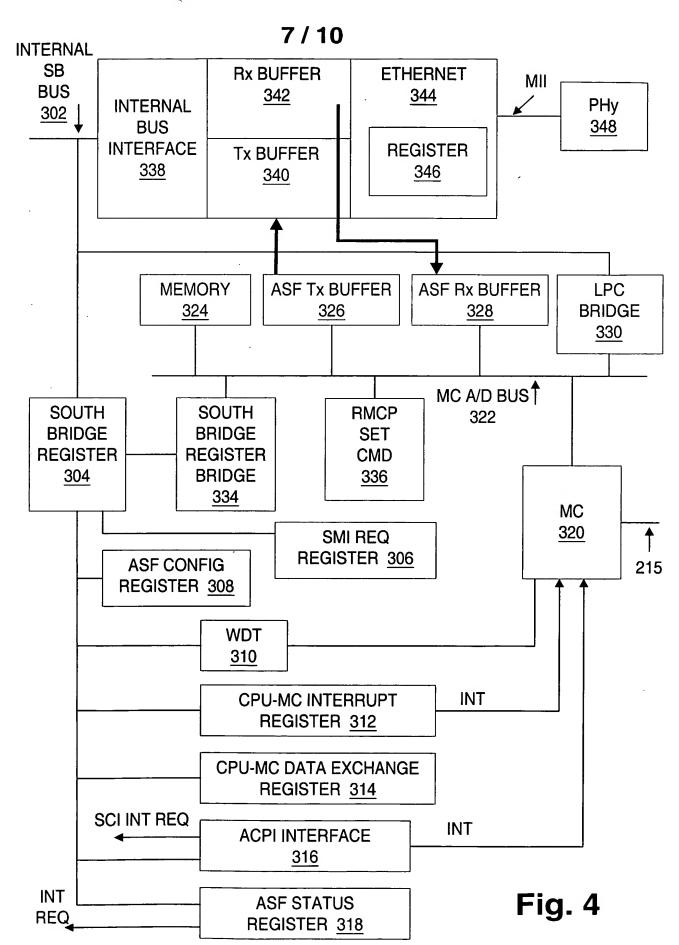


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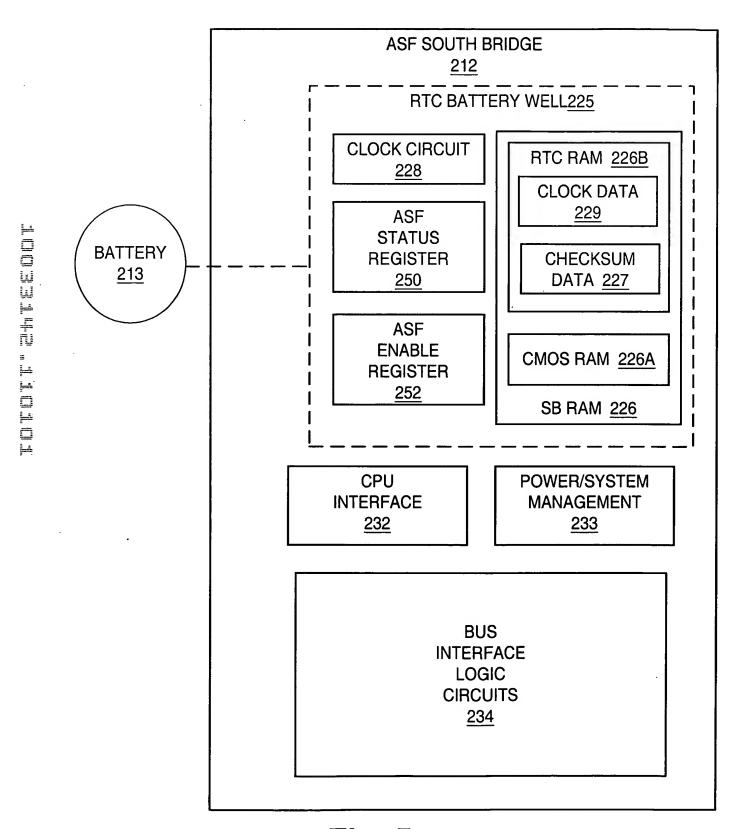


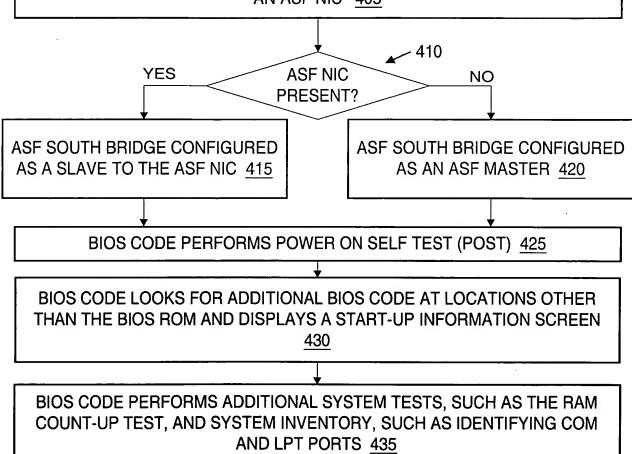
Fig. 5



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THE PROCESSOR JUMPS TO THE BIOS CODE LOCATION IN THE ROM BIOS, COPIES THE BIOS CODE TO RAM, AND PROCESSES THE BIOS CODE INSTRUCTIONS FROM RAM, INCLUDING CHECKING FOR THE PRESENCE OF AN ASF NIC 405



BIOS CODE IDENTIFIES PLUG-N-PLAY AND OTHER SIMILAR DEVICES AND DISPLAYS A SUMMARY SCREEN 440

BIOS CODE IDENTIFIES THE BOOT LOCATION 445

Fig. 6





500

ASF SOUTH BRIDGE IN SLAVE MODE RESPONDS TO REQUESTS FROM THE ASF NIC FOR INTERNAL SENSOR STATUS 505

ASF SOUTH BRIDGE IN SLAVE MODE RESPONDS TO SMBUS POLLS FROM THE ASF NIC $\underline{510}$

Fig. 7A

600

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Fig. 7B